

**Simulation and Characterization of Voltage Follower for Class A topology in CMOS
180nm Technology**

Dhavalsinh S. Ravalji^{*1}, Rajnikant M. Soni²

^{*1}ME Student, ²Assistant Professor, Electronics and Communication Engineering, Gujarat technological university, Laljibhai Chaturbhai Institute of Technology, Bhandu-38412, Gujarat, India

dhavalravalji@gmail.com

Abstract

This paper is about two class-A voltage followers like basic voltage follower and super source follower. Both have their own advantages and limitations. Here using ideal current source and then using a current mirror as a source current analysis done for both basic voltage follower and super source follower. After doing that process results are used to compare the performance of the above voltage followers. All analysis was supported by the simulation results. Various topologies of voltage follower like Basic voltage Follower, Super Source Follower are designed in 180nm technology with $\pm 1.8V$ power supply. These different The analysis are made in terms of gain, bandwidth, offset and Delay using ELDO spice, IC station and Design architect of mentor graphics.

Keywords: Voltage Follower, Basic Voltage follower, Super source follower, current mirror, low resistance.

Introduction

Now days market trend is for low power or low voltage supply for electronic devices. So it is must that the configurations of the devices are according to them. In that, present revision of voltage technology size do not evolve linearly and Threshold Voltage, Saturation Voltage not be reduced linearly. These serious facts limit the voltage swing low voltage supply. Many techniques, such as feedback, independent threshold, pseudo differential, Push-pull symmetric, body resulted have been proposed in the literature to reduce the power requirement while maintaining acceptable performance[2].

Voltage Follower

Voltage Follower is basic circuit, Specially for analog circuits. A voltage buffer amplifier is used to transfer a voltage from a first circuit, having a high output impedance level, to a second circuit with a low input impedance level. In addition, for applications in portable electronics, where life of the battery needs to be extended to the maximum possible, static power consumption of the buffer should be small, while the slew-rate remains high. . The voltage follower circuit mainly used as impedance matching and level shift.

A. Basic voltage follower

Voltage follower is also known as buffer. Unity gain is also a expectation from buffer. $V_{out} = V_{in}$. The voltage follower, also called a buffer, provides a high input impedance, a low output impedance and unity gain. As the input voltage changes, the output and inverting input will change by an equal amount.

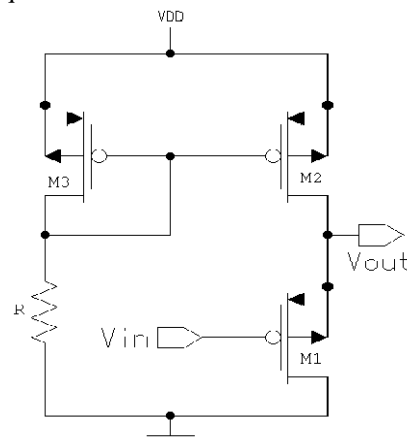


Fig.1 Basic Voltage Follower [1]

Here, the first transistor is totally depended upon the output current, so that the ground to source voltage will be signal depended.

B. Super source follower

To minimize the area and power dissipation required to reach given output resistance in Source Follower, the super source follower Configuration shown in figure 2.

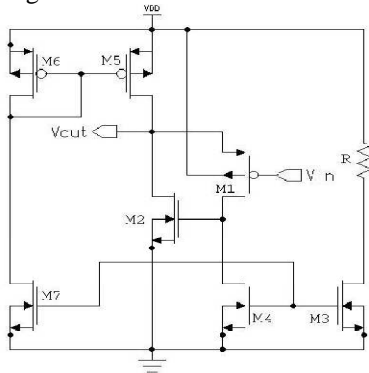


Fig.2 Super Source Follower[1]

This circuit uses negative feedback from M_2 to reduce output resistance. From a qualitative point of view, when the input voltage is constant and the increase in output voltage, the amplitude of the drain current of M_1 is also increasing, in turn, increases the gate-source voltage of the M_2 . Accordingly, the drain current increases in M_2 , thereby reducing the output resistance by increasing the total current that flows into the output node under these conditions.

Simulation Results

All the simulations done in Eldo SPICE in mentor graphics tool with TSMC 180nm technology with 1.8 supply voltage.

A. Result of basic voltage follower

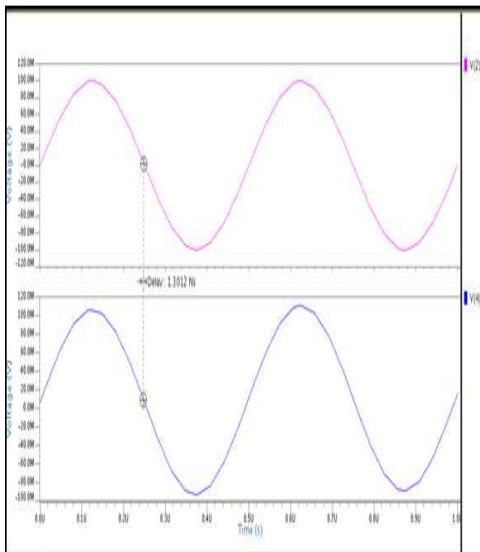


Fig 3. Delay in Basic Voltage Follower
In fig. we could show the delay of BVF is 1.3012 Ns.

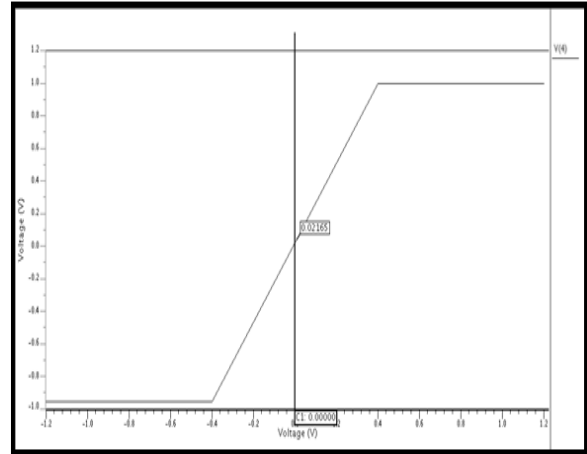


Fig.4 Offset in BVF
In fig. 4 we could show that the offset of Basic Voltage Follower is 21mV.

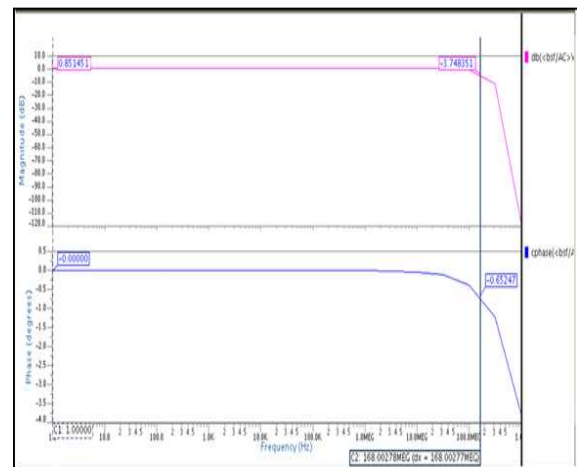


Fig.5 Frequency Response in BVF.

Fig.5 Now, fig. shows the frequency response of basic voltage follower with gain bandwidth product it is 0.85 over 168.00MHz in BVF circuit, result shows the actual performance of the circuit.

B. Result of Super Source Follower

Pre Layout Simulation of Super Source Follower is carried out using Eldo SPICE in mentor graphics tool with 0.18μm process technology at supply voltage $V_{DD} = \pm 1.8V$, $V_{SS} = 0V$. Simulation results are as depicted in figure below. Here, in figure. 6 we give sine wave as an input to catch the perfect working of circuit.

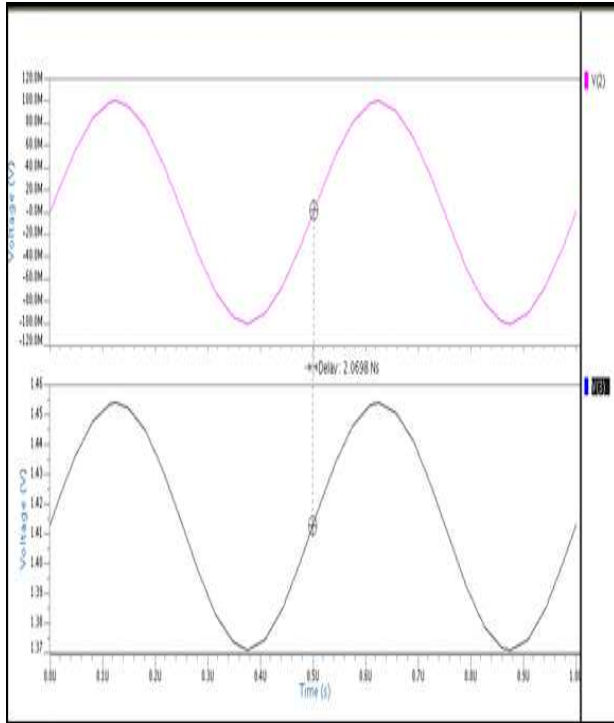


Fig.6 Delay in Super Source Follower.

Delay in the Super Source Follower is 2.069ns

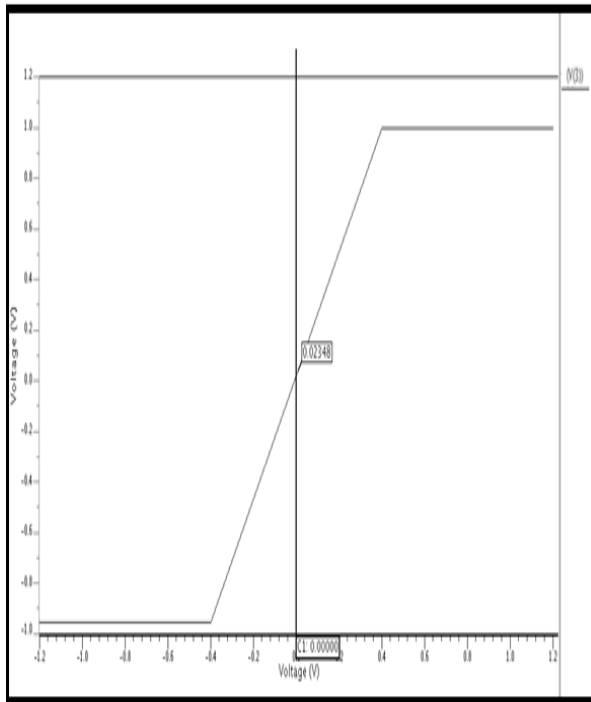


Fig.7, Shows the offset in SSF is 23mV.

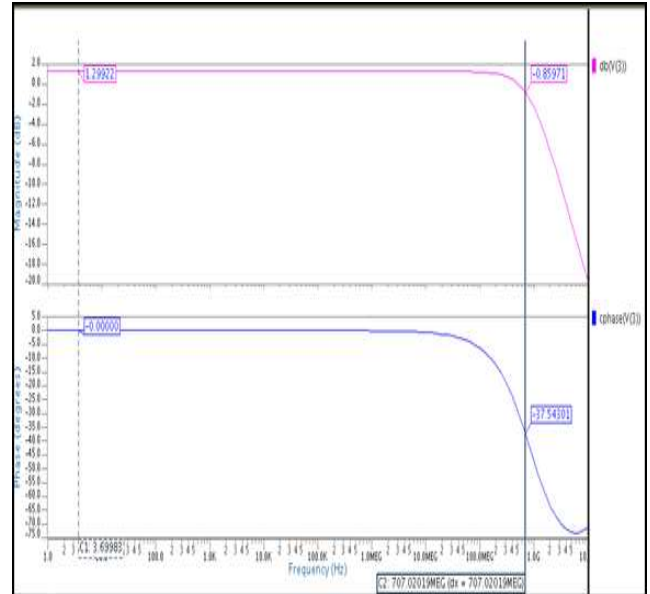


Fig.8 Frequency response for super source follower.

Fig.8 Now, fig. shows the frequency response of Super Source follower with gain bandwidth product it is 1.2 over 707.02MHz in SSF circuit, result shows the actual performance of the circuit.

Results

Table I: Simulated comparison of two class-a topologies of voltage follower

Class Topology	A	Gain (db)	Offset (V)	Bandwidth (MHz)	Delay (Ns)
Basic Voltage Follower		0.85	0.0216	168.00	1.3012
Super Source Follower		1.2992	0.0234	707.021	2.069

Conclusion

The simulation results for class-A voltage follower is presented in this paper in particular one technology 0.18um. The comparison of these technologies has been summarized in Table I. Where the gain, offset, bandwidth and delay is well compared and shows better performance of circuitry.

References

- [1] Gaurang P. Banker, Amisha P. Naik and Dr. N. M. Devashrayee, June 2011: 'Comparative Analysis of Low Power CMOS class-A Voltage Followers with Current Mirror as a Load', *IJECT VOL. 2, ISSN: 2230-7109(online)*.
- [2] P. E. Allen, D. R. Holberg, 2002, "CMOS analog circuit design", Oxford University Press, 2nd edition.
- [3] F. Maloberti, 2003, "Analog Design For CMOS VLSI Systems", Kluwer Academic/Plenum press.
- [4] R. J. Baker, H. W. Li, D. E. Boyce, 2005, "CMOS Circuit Design, Layout and Simulation", IEEE Press Series on Microelectronics Systems.
- [5] Y. Kong, S. Xu, H. Yang, July 2007, "An Ultra Low Output Resistance and Wide Swing Voltage Follower", *ICCCAS 2007*, pp. 1007 - 1010.
- [6] Neeraj Yadav, "Low Voltage Analog Circuit Design Based on the Flipped Voltage Follower", *IJECSE*, vol. 1, no. 2, pp/ 258-273. ISSN.